OPTIMIZATION OF TOTAL REVERSIBLE LOGIC IMPLEMENTATION COST USING VEDIC MATHEMATICS

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Abstract

In every operation of an Arithmetic Logic Unit (ALU), a bit lost is an information lost with the resulting disappation of power and difficulties in recovery of the information. Reversible logic addresses recovery of bits lost by reconstructing the inputs from the gate outputs and reduces power dissipation. Theoretically reversible logic consumes less power which has already been proven using techniques of Vedic mathematics. Multiplication in ALU has more computations which consume more power and also the loss in bits adds to power dissipation. Area optimization can be achieved by implementing a Vedic multiplier with reversible logic. It uses the Vertically and crosswise (Urdhva-Tiryyagbhyam) sutra having a carry save feature, which makes the system efficient. This paper proposes to reduce the Total Reversible Logic Implementation Cost (TRLIC includes the number of gates, quantum cost, constant inputs and garbage output) using reversible logic circuits in existing designs like 2x2 Vedic multiplier and other combinational circuits. This logic can be used in DSP computations, effective ALU designs, and cryptographic algorithms.

Keywords

Vertically and crosswise, Urdhva-Tiryyagbhyam sutra , TRLIC, 2x2 Vedic multiplier.

Introduction

Vedic Mathematics is an ancient and powerful mathematics concept developed by Jagadaguru Shankaracharya Sri Bharati Krishna Tirthaji between 1911and 1958. It includes sixteen sutras dealing with arithmetic, algebra, geometry, trigonometry and calculus. The methods he showed and simple sutras on which it is based are extraordinarily simple and simple to apply. Among the 16 sutras is Vertically and crosswise (Urdhva-Tiryagbhayam) which is a general formula applicable to all cases of multiplying and dividing two numbers of any size.

Implementing the reversible logic gates has the advantage of reducing gate counts, garbage outputs as well as constant inputs and has found its application in several technologies such as low power CMOS, Nano-technology and optical computing. The proposed paper uses the reversible logic concepts for computing 2*2 multiplications.

Literature Review

A. Literature Survey of Reversible Logic Gates

Every bit of information that is lost in the combinational circuit results in dissipations of heat of the order of K*T*ln2 Joules, where K is Boltzmann's constant (1.38*10^-23), T is

Absolute Temperature, which in turn increases the power consumption of the system. This is proved by the second law of Thermodynamics (which states that any irreversible process leads to loss of energy). Charles Bennett showed that if computations were carried out in the Reversible way then the energy dissipation would not occur. Since, in the reversible logic gates, every input vector can be recovered from an output vector there is no loss of information.

B. Optimization Parameter

In the proposed paper the following important parameters are considered:

- Gate Count (GC): This is the Total number of reversible logic gates needed for implementing of reversible circuits
- Quantum Cost (QC): This refers to calculating the number of primitive reversible logic gates required for realizing the circuit
- Constant input (CI): The number of inputs kept constant i.e either at 1 or 0 to realize the required function
- Garbage Output (GO): The number of the outputs of reversible logic gates which are not used for further computations
- Total Reversible Logical implementation Cost (TRLIC): Is the summation of number of Gate counts, Quantum cost, Constant inputs, and Garbage outputs

$$TRLIC = \sum (GC, QC, CI, GO)$$

C. Reversible Logic Gates

A reversible logic gate has a one to one correspondence between input and outputs so it is easy to recover the inputs from the output, also it has equal number of inputs and outputs.
The basic gates considered in this paper are as follows:

1. Feyman Gate: The Quantum Cost of this gate is one (1) and has 2 input 2 output (2x2), which is used for copying the required outputs. The logical circuit diagram as shown in Fig. 1

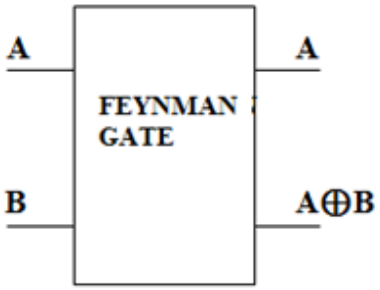


Fig.1 Feynman Gate[1]

2. Peres Gate: The Quantum Cost of this gate is four (4). It is a 3 input, 3 output (3x3) reversible logic gate. It is also called as New Toffoli gate because it is made up of using one Toffoli gate and one Feynman gate, the logical circuit diagram as shown in Fig. 2.

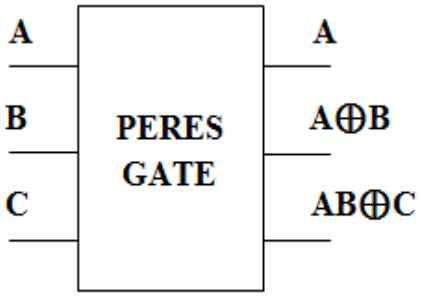
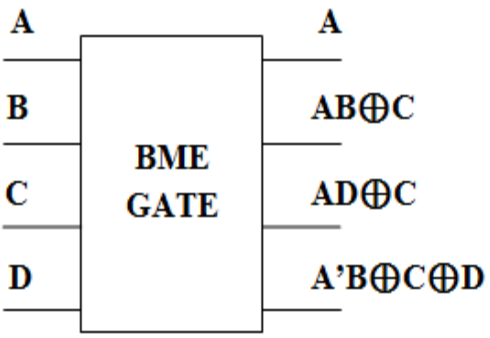


Fig.2 Peres gate[1]

3. BME Gate: The Quantum Cost of this gate is five (5) and it is a 5 input, 5 output (5x5) reversible gate. The logical circuit shown in Fig. 3.



a.

Fig.3 BME gate[1]

Urdhva-Tiryagbhyam Multiplication Algorithms

From the sixteen sutras which are there in Vedic mathematics, the Urdhva-Tiryyagbhyam and Nikhilam sutras are used for Multiplication. The Nikhilam sutra is best used for multiplying numbers close to a power of 10. The UT sutra gives a general method for multiplication and is based on the generation of partial products and then these partial products are added concurrently.

1. UT Algorithm:

This algorithm can be explained by considering two multiplicands (a1, a0) and two multiplier (b1 b0) which results in four bits after multiplication. The line diagram of 2x2 Vedic multiplications is shown in Fig. 4.

Steps to be followed for computing 2x2 multiplications:

1. To get the LSB (Least significant bit) of the final result, First Vertically multiply the LSBs of multiplicand and multiplier.
2. To get the second bit of final result, the LSB of the multiplicand is multiplied with MSB (Most significant bit) of the multiplier and the MSB of the multiplicand is crosswise multiplied with LSB of the multiplier.

3. To get the resultant sum and carry (third and fourth bit of final result) vertically multiply MSBs of the multiplicand and multiplier. These products are added with the previous carry obtained in the step (2).

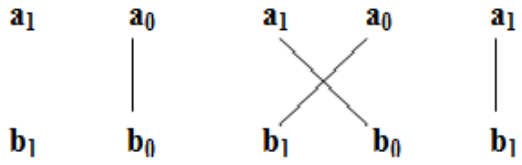


Fig.4 2x2 Vedic multiplication[1]

2. Design

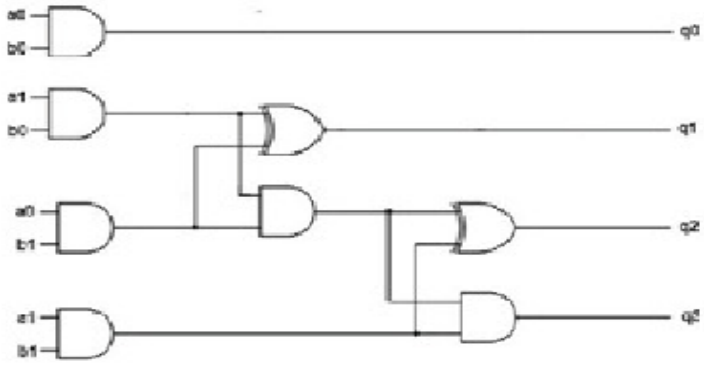
Consider the two binary multiplicands (a1 a0) and multipliers (b1 b0) as giving four results, q0, q1, q2, and q3, after multiplication. The 2x2 Vedic multiplications using UT is based the following Four Equations and also shown in Fig. 5.

q0= a0*b0……(1)

q1= (a1*b0) XOR (a0*b1)……. (2)

q2= (a0*a1*b0*b1) XOR (a1*b1)……. (3)

q3= (a0*a1*b0*b1)…… (4)



qqs

Fig.5 2x2 Binary Vedic multiplier[3]

The Existing design [1], proposed by Gowthami. P and R V S Satya Narayana for the Reversible 2x2 Vedic multiplier, consists of 5 different reversible gates and include 1 BVF, 2 BME, 1 Peres and 1 Feynman gates. The Quantum cost of this design is 19 and TRLIC is of 33. Their design as shown in Fig. 6.

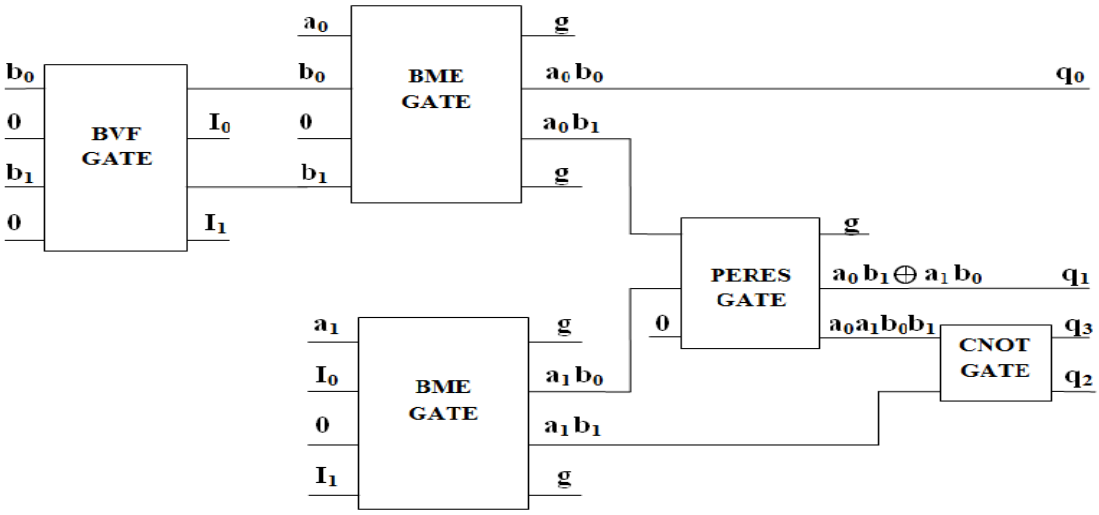


Fig.6 Existing Design[1]

The next existing design [2], proposed by Sonali S. Kothule, Govind U. Kharat, Shekhar H. Bodake for the Reversible 2x2 Vedic multiplier design, consists of 5 reversible gates and include 5 Peres and 1 Feynman gates. The Quantum cost of this design is 21 and TRLIC is of 40. Their design as shown in Fig. 7.

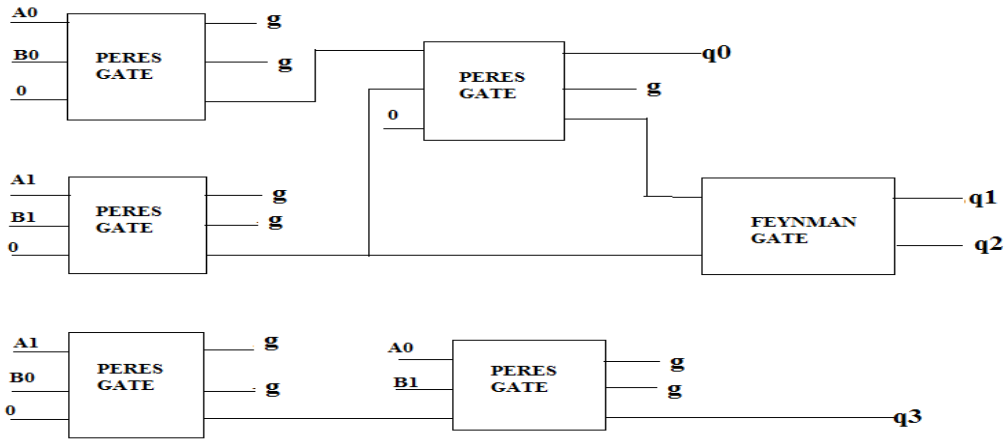


Fig.7 Existing Design[2]

The Optimized design of a 2x2 UT multiplier using Reversible gates is shown in the Fig. 8. It consists of 4 number of gates and includes 2 BME, 1 Peres and 1 Feynman gate. The Quantum cost of this design is 17 and TRLIC is 29.

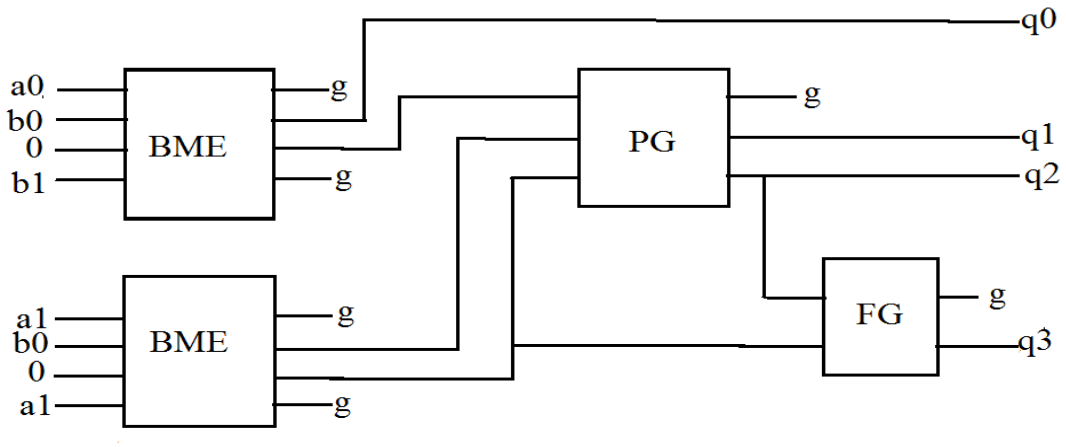


Fig.8 Proposed Design

Results

The design of a 2x2 Vedic multiplier using the UT sutra is simulated using Xilinx ISE 14.2. The simulated design is verified for test cases and the waveform is shown figure 9. The multiplier is extended to 4x4, 8x8 and 16x16 multipliers. The simulated design of the 16x16 multiplier is shown in figure10.

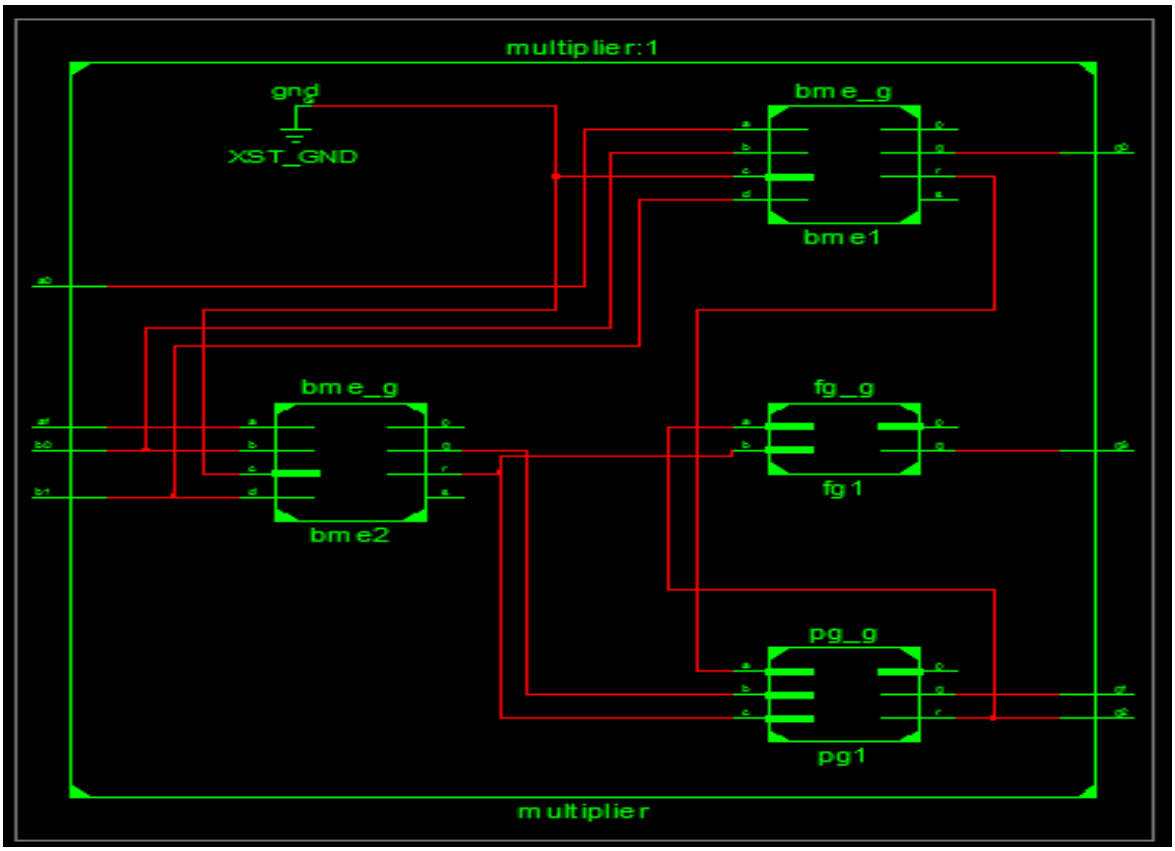


Fig 9 Schematic of 2x2 Vedic Multiplier

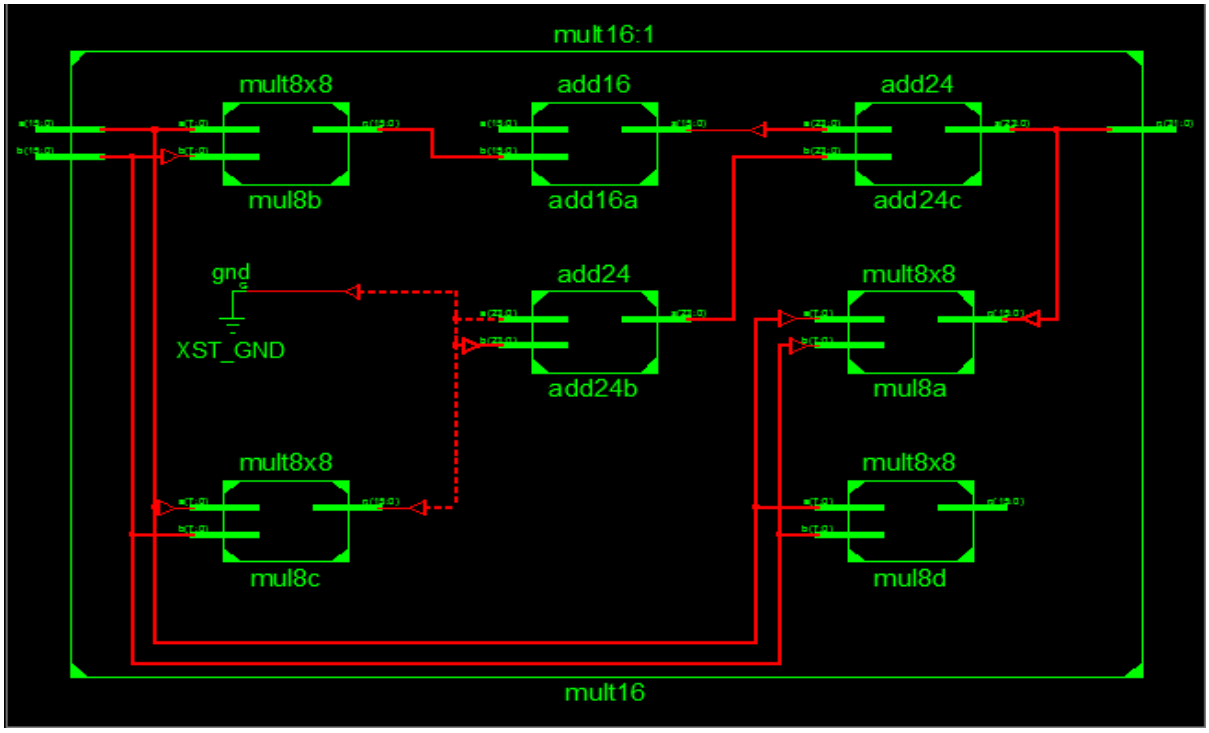


Fig10. Schematic of 16x16 Vedic multiplier

The test bench result of 16x16 multiplier is shown in figure 11.

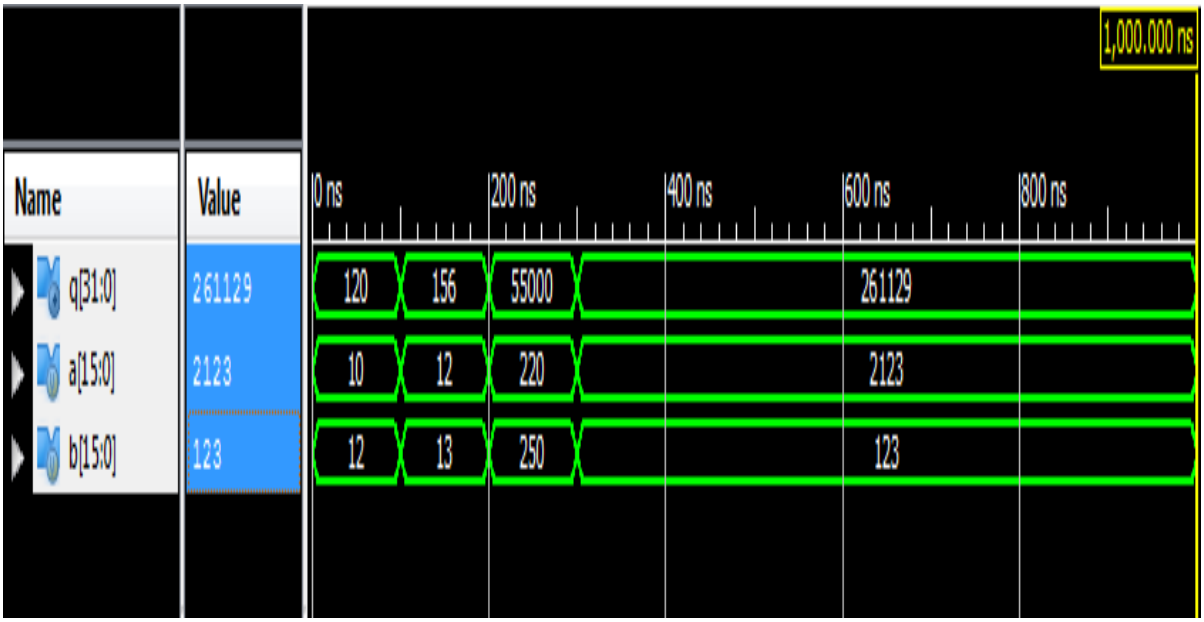


Fig 11 Test bench result 16x16 multiplier

A comparison of the proposed 2x2 Vedic multiplier design with existing designs is shown below.

Table 1 Comparison Table of 2x2 multiplier

Parameters	2x2 Multipliers		
	Proposed design	Existing Design [1]	Existing Design [2]
Number of gates	4	5	6
Constant Inputs	2	5	4
Garbage Outputs	6	5	9
Quantum Cost	17	19	21
TRLIC	29	34	40

The TRLIC of proposed 2x2 Vedic multiplier is optimized in comparison with existing designs [1] and [2].

Conclusion

In the proposed design, the Urdhva Tiryakbhyam 2x2 Vedic multiplier is designed using reversible logic gates. The Total Reversible logic Implementation Cost of the multiplier is optimized. The quantum cost, constant inputs, garbage outputs and number of gates are also optimized when compared to existing designs. The 2x2 multiplier is extended to 4x4, 8x8 and 16x16 multiplication and the TRLIC of higher bit multipliersis also minimized.

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